REMARKS

This Amendment is responsive to the Official Action mailed on February 27, 2004. The Office Action rejected claims 23 and 26 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (U.S. patent number 5,509,134) and rejected claims 24-25 under 35 U.S.C. 103(a) as being unpatentable over Fandrich in view of Kishi et al. (U.S. patent number 4,841,432) or Noel et al. (U.S. patent publication 2002/00168891). The Office Action rejected claim 17 under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (U.S. patent number 5,418,752) in view of Kaki et al. (U.S. patent number 5,809,515), with dependent claims 18-22 further rejected in view of Kishi or Noel. The Office Action also repeated its previous rejected based on an insufficient showing of conception and reduction to practice. The present Amendment has cancelled claim 23, rewritten claims 24 and 25 in independent form, changed the dependency of claim 26, and added new claim 27. For the reasons given below, it is respectfully submitted that various rejections of the pending claims are in error and should be withdrawn.

Previously filed Declaration was *not* filed to show a Reduction to Practice, but to show that "the invention was not known or used by *others*"

In paragraphs 2-5, the present Office Action states that the Declaration filed with the previous Amendment is insufficient to establish conception and a reduction to practice of the present invention. It is respectfully submitted that purpose of this Declaration has been misunderstood: the Declaration was *not* submitted for purposes of establishing conception and a reduction to practice, but rather to show the MultiMediaCard System Specification Version 1.4, MMCA Technical Committee is *not applicable as prior art under 35 U.S.C. 102(a)*.

More specifically, 35 U.S.C. 102(a) states: "A person shall be entitled to a patent unless (a) the invention was known or used by <u>others</u> ...", where the underlining is added. The previous Office Action rejected claims 17-26 are either rejected under 35 U.S.C. 102(a) as being anticipated by the MultiMediaCard System Specification Version 1.4, MMCA Technical Committee, or rejected under 35 U.S.C. 103(a) with the MultiMediaCard System Specification Version 1.4 as a secondary reference. The Declaration included with the previous Amendment under 37 CFR 1.132 states that the relevant portions of "The MultiMediaCard System Specification" of the MMCA Technical Committee, Version 1.4, are a *publication of the Applicants' own invention*. As such, the material is *not applicable as*

prior art under 35 U.S.C. 102(a) and the rejection of claims 17-26 is accordingly traversed as "the invention was not known or used by *others* ... before the invention thereof by the applicant for patent", in the language of 35 U.S.C. 102(a) (emphasis added).

It is respectfully submitted that the previously submitted Declaration is sufficient for the purposes for which is was submitted, namely to show the MultiMediaCard System Specification Version 1.4, MMCA Technical Committee is not applicable as prior art. Consequently, the previous Office Action's rejection of the pending claims, which is repeated in pages 10-14 of the current Office Action, based on this reference is improper and should be withdrawn.

If the Examiner has any questions related to this Declaration or its use, a call to the undersigned is invited.

(Additionally, it is noted that pages 10-14 of the current Office Action repeat the rejections of claims 23-26 based on Harari, the response to which is not noted in the current Office Action. As described further in the previous Amendment, the cited portions of Harari are concerned with enabling of an erase process. These rejections are respectfully submitted to be in error as these claims drawn to a *write* process, not an *erase*, and is about *protecting* groups of cells for this process, not *enabling* them.)

Objection to claim 17

The Office Action objected to claim 17 due to the stray "15" that was present in its last element. The Examiner is thanked for noting this error, which has now been corrected. Claim 17 maintains its designation as "Original" despite this change, as the "15" was due to a corruption of the text and its removal restores claim 17 to the form in which it was originally presented when the parent of the present application was filed.

New Grounds for Rejection of claims 17-22

The Office Action introduced new grounds for the rejection of claims 17-22, with claim 17 rejected under 35 U.S.C. 103(a) based on Harari in view of Kaki, and with dependent claims 18-22 further rejected in view of Kishi or Noel. It is respectfully submitted that these rejections are not well founded and should be withdrawn.

The Office Action is correct in that Harari presents a memory having a plurality of sectors and using a corresponding plurality of sectors tags to indicate whether the memory cells in the corresponding memory sector are erasable when the tags are set and any

combination of memory sectors can be simultaneously erased. The Office Action then relies upon Kaki to supply the missing elements, base upon the proposition that it would be obvious to combine these references for this purpose. Rather, it is respectfully submitted that the Office Action's use of Kaki is incorrect and that, in contrast, Kaki teaches away from the aspects of the present invention presented in claim 17.

Kaki is primarily interested in improving write performance, which it does by distributing a given write across several differ memory chips, but it also has some discussion of erase processes in the portion cited to which the Office Action refers.

The cited portion of Kaki (column 7, line 64, through column 8, line 14) generalizes the discussion of the preceding paragraph (beginning at column 7, line 32). The cited portion of Kaki states that the erase process described in the preceding discussion is changed according to erase structure used by flash memory; that is, it states that flash memories being used will have a specified unit of erase and that the techniques of the preceding paragraph have to conform with this unit of erase. In the preceding paragraph (beginning at column 7, line 32), this unit of erase is the sector, while in the cited portion (column 7, line 64, through column 8, line 14) the unit of erase is a whole chip. According to Kaki, what the Office Action identifies as "tags" correspond, and can only correspond, to specific unit of erase in the flash architecture. Kaki neither teaches nor suggests the use of two levels of tags for both the basic unit of erase (such as a sector) and the composite, multi-sector unit of the group. Instead, according Kaki, "tags" must correspond to the specific architecture's unit of erase: either sector tags, or rather what the Office Action is identifying as tags, or group tags, but not both.

The teachings of Kaki are also restrictive as to the combinations of erase units that can be set for erasing together. As described at column 7, lines 41-42, "areas to-be-erased are set *so as to be in different memory chips* of the flash memories 4", where the emphasis has been added. Consequently, Kaki only allows for one unit of erase per chip to set for erase together, whether the appropriate "area to-be-erased" is a sector or a whole chip. (This is similar to the arrangement used in Kaki for writing, which is the main subject of the patent, where a write is distributed across the separate chips.)

Further, Kaki specifies that the erase of the units of erase are erased sequentially, not simultaneously. This is shown in Figure 4 of Kaki and is based on the loop in step 45, as described at column 7, lines 49-50: "Subsequently, the processor 2 determines if the next area

to-be-erased exists (step 45)." So that rather than simultaneously erasing all of the units of erase set for erase, Kaki teaches that a sequential process must be used.

Therefore, according to Kaki, an erase process is based on, and only on, the specific unit of erase in the particular flash memory chip with no indication of other size of erase or combination of differing sizes; requires a very specific and limited setting of the erase structures to erased together; and performs the erases sequentially. Thus not only is there no suggestion of tagging for erase a composite structure of multiple units of erase, being able to select any combination of either units of erase or composite units (or "groups") for erase, or performing the erase of these selected structures simultaneously, but Kaki instead teaches away from all of there.

In contrast, the aspects of the present invention presented in claim 17 uses two levels of structure, the sector and the group, with corresponding tags

> wherein all the memory cells belonging to one memory sector are erasable
> when either the corresponding sector tag or the corresponding group tag of the
> memory sector is set;

Further, it specifies that any combination of sectors or groups can be tagged for erase and erased simultaneously:

> wherein *any combination of memory sectors* in a memory group be
> *simultaneously erased, and any combination of the memory groups* can be
> *simultaneously erased.*

Thus, claim 17 contains a number of aspects from which Kaki teaches away.

Consequently, it is believed that a rejection of claim 17 and its dependent claims, claims 18-22, under 35 U.S.C. 103(a) based on Harari in view of Kaki is not well founded and should be withdrawn. It is respectfully submitted that not only is it is not obvious to combine these two references in the manner recited in the claims, but that the Office Action is improperly combining the two references in a manner gained by hindsight of the present invention and in a manner that is explicitly contrary to the teachings of Kaki.

Dependent claims 18-21 are rejected based on Harari in view of Kaki, and further rejected in view of Kishi or Noel, and are consequently believed allowable for the reasons stated above with respect to claim 17. They are further believed allowable for as is it believed that further rejections based on either Kishi or Noel are also not well founded.

First, considering Kishi, with respect to claims 18 and 20, the Office Action states that "Kishi discloses the number of memory sectors in each memory group is configurable (abstract) for the purpose of optimizing flash devices" and that "Kishi discloses the number of

memory cells in each memory sector is configurable (abstract) for the purpose of optimizing flash devices." It is respectfully submitted that both of these statements are incorrect.

The Kishi patent is entirely directed at the reconfiguration of *tapes* for controlling machine tools. It discusses flash devices neither in the abstract nor, as far as can be determined, in the rest of the patent. More specifically, it provides no discussion of "optimizing flash devices" in any form, as stated in the Office Action. Kishi is instead concerned with a very different technology. In particular, there appears to be no disclosure of a memory system where "the number of memory cells in each memory sector is configurable"---or, for that matter, even the use of memory cells themselves in the technology of Kishi. There also appears to be no disclosure of a memory system where "the number of memory sectors in each memory group is configurable."

Consequently, it is respectfully submitted that a further rejection of claims 18 and 20 based on Kishi is not well founded and should be withdrawn. It is believed neither obvious to combine Kishi with the other references nor how to do so as the tape memory of Kishi is a very different technology having a different structure from the sort of memory based on cells and sectors found in the claims.

Claims 19 and 21 respectively depend upon claims 18 and 20 and are believed allowable for the reasons stated above with respect to those claims. Additionally, with respect to claims 19 and 21, the Office Action respectively states "Kishi further discloses the corresponding sectors in each memory group is calculated in real time (col.5 lines 32-42)" and "Kishi further discloses the corresponding cells in each memory sector is calculated in real time (col.5 lines 32-42)." As already noted, Kishi is dealing with a very different technology that would not be obvious to combine with the other reference and which is not based on cells and sectors found in the claims. Consequently, whatever Kishi is up to in the cited location (column 5, lines 32-42), it is neither calculating "number of memory cells in each memory sector" nor "the corresponding sectors in each memory group". Consequently, claims 19 and 21 are further believed allowable for these reasons.

Considering the alternate further rejections based on Noel, with respect to claims 18 and 20, the Office Action states that "Noel discloses the number of memory sectors in each memory group is configurable (block 265) for the purpose of optimizing flash devices" and that "Noel discloses the number of memory cells in each memory sector is configurable (block 265) for the purpose of optimizing flash devices." It is respectfully submitted that both of these statements are incorrect.

The Noel application is directed at multiprocessor computer architectures in which processors and other computer hardware resources are grouped into partitions. Specifically, it divides a single physical machine into separate logical partitions to act as independent processors. The cited location (block 256) is related to a software configuration and mentions memory only to describe the relative privileges that the various logical partitions have to the processors' memory. Noel discusses flash devices neither in this location nor, as far as can be determined, in the rest of the patent. More specifically, it provides no discussion of "optimizing flash devices" in any form, as stated in the Office Action. Noel is instead concerned with a very different set of problems and technologies. In particular, there appears to be no disclosure of a memory system where "the number of memory cells in each memory sector is configurable"---or, for that matter, even the use of memory cells themselves in the teachings of Noel, as it is concerned with the logical partitions of a machine into independent processors. There also appears to be no disclosure of a memory system where "the number of memory sectors in each memory group is configurable."

Consequently, it is respectfully submitted that the alternate further rejection of claims 18 and 20 based on Noel is also not well founded and should be withdrawn. It is believed neither obvious to combine Noel with the other references nor how to do so as the concerns of Noel a very different subject related to multiprocessor computer architectures and having nothing to do with memories based on cells and sectors found in the claims.

Claims 19 and 21 respectively depend upon claims 18 and 20 and are believed allowable for the reasons stated above with respect to those claims. Additionally, with respect to claims 19 and 21, the Office Action respectively states "Noel further discloses the corresponding sectors in each memory group is calculated in real time (block 256)" and "Noel further discloses the corresponding cells in each memory sector is calculated in real time (block 256)." As already noted, Noel is dealing with a very different technology that would not be obvious to combine with the other reference and which is not concerned with cells and sectors as found in the claims. Consequently, whatever Noel is up to in the cited location (block 256), it is neither calculating "number of memory cells in each memory sector" nor "the corresponding sectors in each memory group". Additionally, Noel states that "it is possible to dynamically change partitions", but gives no description of doing this "in real time". Consequently, claims 19 and 21 are further believed allowable for these reasons.

New Grounds for Rejection of claims 23-26

The Office Action also introduced new grounds for the rejection of claims 23-26. Claim 23 has been cancelled at this time, with formerly dependent claims 24 and 25 rewritten in independent form. Claim 26 has had its dependence changed to claim 24 and new claim 27 is the same as claim 26, except for instead depending upon claim 25. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) based on Fandrich in view of Kishi or Noel. It is respectfully submitted that these rejections are not well founded and should be withdrawn.
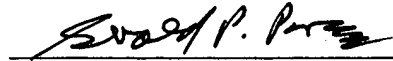
As is described above with respect to claims 18-21, both of Kishi and Noel are directed to very different technologies than that of Fandrich. It is again respectfully submitted that it would not be obvious to combine such diverse technologies for the purposes of the claims. Further, neither of these supplemental references describes either of the specific further limitations of "wherein the number of memory cells in each memory group is configurable" or "wherein the corresponding cells in each memory group are calculated in real time".

Consequently, it is believed that a rejection of claims 23-26 based on Fandrich in view of Kishi or Noel is not well founded and should be withdrawn.

Conclusion

Therefore, for any of the above reasons it is respectfully submitted that a rejection of claims 17-21 and 23-26 under the stated reasons is not well founded and should be withdrawn. Reconsideration of claims 17-21 and 23-26, along with consideration of new claim 27, and an early indication of their allowance are respectfully requested.

Respectfully submitted,

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